## AMENDMENTS TO THE SPECIFICATION

Please replace the paragraphs of the specification as identified below with the their respective amended paragraphs rewritten in amendment format:

Page 22, lines 16-23:

The barrier layer and the sheet layer are formed using, for example, an IMP (ion metal plasma) method, or a PVD (physical vapor deposition) method such as vacuum deposition, sputtering, or ion plating. The undercoat film sufficiently covers the step between an electrode pad 14 and the insulating film 18, and is formed continuously over the electrode pad 14 and the insulating film 18 (including the inside of the hole portion H3). Moreover, the thickness of the barrier layer that forms the undercoat film is, for example, approximately 100nm~~μm~~, and the thickness of the sheet layer is, for example, approximately several hundred μm.

Page 34, lines 14-23:

When the steps described above have been completed, the stacked semiconductor chips C3 and C4 are disposed in a reflow apparatus, the lead free solders provided on the distal ends of the connecting terminals 36 formed on the semiconductor chips C3 and C4 are melted, and the connecting terminals 36 formed on the semiconductor chip C3 and the connecting terminals 36 formed on the semiconductor chip C4 are bonded (bonding step). As shown in Fig. 12, the distal ends of the connecting terminals 362~~0~~ formed on the semiconductor chip C3 ~~C1~~ on the back surface side (the semiconductor chip C4 side) have a concavo-convex shape, the

bonding strength increases because the bonding area of the lead free solder 38 is large, and thereby it is possible to implement an improvement of the reliability.

Page 41, lines 2-11:

When the steps described above are completed, the stacked semiconductor chips C5 and C6 are disposed in a reflow apparatus, the lead free solders provided on the distal ends of the connecting terminals 46 formed on the semiconductor chips C5 and C6 are melted, and the connecting terminals 46 ~~20~~ formed on the semiconductor chip C5 and the connecting terminals 46 formed on the semiconductor chip C6 are bonded (bonding step). As shown in Fig. 17, the distal ends of the connecting terminals 46 formed on the semiconductor chip C5 on the back surface side (the semiconductor chip C6 side) have a curved surface, the bonding strength increases because the bonding area of the lead free solder 48 is large, and thereby it is possible to implement an improvement of the reliability.